REMARKS

Favorable reconsideration of this application in view of the above amendments and the following remarks is respectfully requested. Claims 1 and 10 have been amended to correct inadvertent typographical errors. Claims 4 and 13 have been amended to further distinguish the subject matter of the instant application. Currently, claims 1 – 18 are pending of which claims 1, 4, 10, and 13 are independent.

The Examiner has rejected claims 1, 2, 4 – 7, 9 – 11, 13 – 16, and 18 under 35 U.S.C. §102(b), has rejected claims 3, 12, and 16 under 35 U.S.C. §103(a), and has objected to claims 8 and 17 as being dependent on a rejected base claim (these claims being allowable if rewritten in independent form). The Examiner's indication of allowable subject matter (claims 8 and 17) is appreciated. In addition, favorable reconsideration of the subject application is respectfully requested in view of the following remarks.

Initially, this application claims priority under 35 U.S.C. §119 from German Application No. 10310140.3, filed March 7, 2003. Applicants supplied a certified copy of priority document No. 10310140.3 on June 17, 2004 (with the Response to the Notice to File Missing Parts), as evidenced by a date-stamped filing receipt, a copy of which is attached. Accordingly, formal acknowledgement of Applicants' claim for foreign priority under 35 U.S.C. §119 is respectfully requested.

Claims 1, 2, 4 – 7, 9 – 11, 13 – 16, and 18 were rejected under 35 USC 102(b) as anticipated by El Ayat et al. (U.S. Patent No. 5,528,600 (hereinafter El Ayat)). The Examiner

takes the position that the El Ayat patent discloses all the features recited within these claims. This rejection is respectfully traversed since the El Ayat patent does not disclose, teach, or suggest the features recited in claims 1, 4, 10, and 13 of using the same control signal SCAN to select a row of integrated modules and to activate a switching transistor to connect the address and command terminals of the integrated modules of the selected row to the address and command bus.

Briefly, the present invention is directed to a test apparatus for testing integrated modules and a method for operating such a test apparatus. Referring to FIG. 1, it can be seen that connection locations **11 - nk**, by which an integrated module **DUT** may be connected to a test unit **2**. The test unit **2**, in turn, is connected to a carrier substrate **1**. The connection locations **11 - nk** form a connection array constructed in the form of a matrix in columns **S1 - Sk** and rows **R1 - Rn**. The connection locations **11 - nk** are arranged in groups wherein each row **R1** (integrated modules **11**, . . . , **1k**) to **Rn** (integrated modules **n1 - nk**) forms its own group. Each of the integrated modules has a control terminal **CS**, an address and command terminal **A/C** and a data terminal **DQ**. An integrated module **DUT** is selected for a test by driving its control terminal **CS** with a control signal SCAN. The control terminals **CS** of connection locations of a respective row **R1 - Rn** is each connected to a control bus SCAN-1 to SCAN-n assigned to this row. The address and command terminals **A/C** of the connection locations of a row **R1 - Rn** can be connected to a common address and a command bus **CMD/ADD** via a respective switching means **T1** to **Tn**.

The switching means **T1** to **Tn** is controlled by a control signal on the respective control bus SCAN-1 to SCAN-n assigned to the row. If, for example, integrated modules **11** to **1k** arranged in row **R1** have to be tested, their respective control terminals **CS** are driven by control signal SCAN-1 on control bus SCAN-1. The control signal SCAN-1 also activates switching transistor **T1** to connect the command and address terminals of the integrated modules arranged in row **R1** to the common command and address bus **CMD/ADD**. All other integrated modules arranged in rows **R2** to **Rn** and their respective switching transistors **T2** to **Tn** are deactivated by respective control signals SCAN-2 to SCAN-n on their corresponding control buses SCAN-2 to SCAN-n.

Consequently, via the control signal SCAN, a row of integrated modules is selected for a test and the *same* control signal SCAN also activates the switching transistor **T**, which connects the selected integrated modules of the selected row to the address and command bus **CMD/ADD**. The SCAN signal selects addresses and commands for the active integrated modules, with the result that the load on the corresponding drivers can be reduced. Due to this technique, selected modules can be operated at a higher frequency or the number of modules per burn-in board can be increased (*see* p 6, line 12 to p 8, line 8).

El Ayat is directed to testability circuits for logic arrays. Referring to FIG. 1 of El Ayat, the function circuit modules **12a - 12i** are arranged in a plurality of rows and columns. A function module whose output is to be controlled is selected by addressing the selected module via an X select line (XSEL) and a Y select line (YSEL). There is one XSEL line associated with

each row of function modules and one YSEL line associated with each column of function modules in array **10**. In a control mode, YSEL lines **22**, **24**, and **26** are controlled by transistors **34**, **36**, **38**, and **40**. The selection of which YSEL line for controllability is achieved by activating the one of column address lines **46**, **48**, or **50** associated with the selected column, and simultaneously activating CM line **44** (*see* col. 5, lines 17 to 21).

In an observe mode, a row-select (RSEL) signal is presented on one of a plurality of row-select lines associated with the row in the array from which the output data is to be read. The same YSEL lines **22**, **24**, and **26**, which are used to select a function module during control mode, are used in the observe mode as output sense lines to observe the output of the function module. The selection of which column line YSEL to observe when the RSEL line associated with a particular row is active is made by using transistors **52**, **54**, and **56**, which are connected between their respective column YSEL lines and a common sense line **58** (*see* col. 5, lines 31 to 53).

The rejection asserts the El Ayat control buses XSEL1 - XSEL3 for operating and driving the modules **12a-12i** are identical to the control buses SCAN-1 to SCAN-n for selecting integrated modules **11-nk** of the present invention. In addition, the rejection equates the address and command bus **46**, **48**, and **50** as well as the respective switches **34**, **36**, and **38** of the El Ayat patent to the address and command bus **CMD/ADD** and the switching means **T1** to **Tn** of the present invention. The El Ayat X select line XSEL is used to select a row within array **10** and the Y select line YSEL is used to select one of the function circuit modules in the selected row.

However, each of the transistors **34**, **36**, and **38** that is used to control YSEL lines **22**, **24**, and **26** are activated/deactivated by a column address signal on the column address lines **46**, **48,** and **50**, which is *different* from the row address signal XSEL. In contrast, the control bus of the instant invention is driven by a control signal to simultaneously (1) operate and drive modules of a number of groups of connection locations and (2) activate a respective switching means connected to the driven group of connection locations. That is, the control signal SCAN used to select a row of integrated modules is also used to activate a switching transistor **T** to connect the address and command terminals of the integrated modules of the selected row to the address and command bus **CMD/ADD**. This is in contrast with the El Ayat patent, where, as explained above, each of the transistors used to control the YSEL lines is activated/deactivated by a column address signal on the column address lines that is different from the row address signal XSEL. Thus, the El Ayat patent does not disclose the feature that the control terminals of the connection locations for selecting the integrated modules for a test are connected to a control bus, and that the address and command terminals of the connection locations are connected to an address and command bus via a respective switching means controlled by the control bus.

Since the El Ayat patent does not disclose, teach, or suggest the features recited within original independent claims 1 and 10 and amended claims 4 and 13 as discussed above, these claims are considered to be in condition for allowance. Claims 2, 3, 5 – 9, 11, 12, and 14 – 18 depend, either directly or indirectly, from independent claims 1, 4, 10, and 13 and, therefore, include all the limitations of their parent claim. These dependent claims are considered to be in

condition for allowance for substantially the same reasons discussed above in relation to their parent claim and for further limitations recited in the claims.

Claims 3, 12, and 16 have been rejected under 35 U.S.C. §103(a) as being unpatentable over El Ayat in view of Boardman (U.S. Patent No. 5,682,472). The Examiner takes the position that it would be obvious to modify the El Ayat integrated circuit with the burn-in board taught by the Boardman patent. This rejection is respectfully traversed. Initially, claim 3 depends from independent claim 1, claim 12 depends from independent claim 10, and claim 16 depends from independent claim 13. Each of these dependent claims includes all the limitations of its parent claim; consequently, each dependent claim is considered to be in condition for allowance for substantially the same reasons discussed above in relation to its parent claim and for further limitations recited in the claim. As discussed above, El Ayat does not disclose the features of independent claims 1, 4, 10, and 13 that the control terminals of the connection locations for selecting the integrated modules for a test are connected to a control bus, and that the address and command terminals of the connection locations are connected to an address and command bus via a respective switching means controlled by the control bus. The Boardman patent, moreover, does not compensate for the deficiencies of the Morison patent and similarly, does not disclose, teach, or suggest these features.

In view of the foregoing, Applicants respectfully request the Examiner to find the application to be in condition for allowance with claims 1 – 18. However, if for any reason the Examiner feels that the application is not now in condition for allowance, he is respectfully

requested to call the undersigned attorney to discuss any unresolved issues and to expedite the disposition of the application.

It is believed that no fees are required at this time. However, Applicants hereby petition for any extension of time that may be necessary to maintain the pendency of this application. The Commissioner is hereby authorized to charge payment of any additional fees required for the above-identified application or credit any overpayment to Deposit Account No. 05-0460.

Respectfully submitted,

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